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1. (Currently Amended) A unidirectional low capacitance transient voltage suppressor ("TVS"), comprising:

a TVS p-n junction diode element;

a low-capacitance ("LC") PIN or NIP diode element; and

the TVS p-n junction diode element being placed in series with opposite polarity to the LC PIN diode.

2. (Original) The circuit of Claim 1, wherein the PIN or NIP diode has an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region; and

the "I" region is located between the p region and n region.

3. (Original) The circuit of Claim 2, wherein the "I" region of the PIN or NIP diode has a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

4. (Original) The circuit of Claim 2, wherein the PIN or NIP diode has a circular-die structure.

5. (Original) The circuit of Claim 2, wherein the PIN or NIP diode has a square die structure.

6. (Original) The circuit of Claim 2, wherein the PIN or NIP diode has a rectangular die structure.

7. (Original) The circuit of Claim 1, adapted to clamp high-voltage transients of either polarity to a predetermined level.

8. (Original) The circuit of Claim 1, wherein the use of the PIN or NIP diode minimizes parasitic losses and signal-line distortion.

9. (Original) The circuit of Claim 1, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

10. (Original) The circuit of Claim 9, operable to reduce the complexity of impedance matching within a high frequency circuit.

11. (Original) The circuit of Claim 9, operable to lower the clamping voltage performance of TVS with capacitances in the range of about 1 pF to 100 pF.

12. (Original) The circuit of Claim 1, in combination with a low parasitic package, operable to reduce capacitances to less than 1 pF.

13. (Original) The circuit of Claim 1, for use in multiple diode arrays.

14. (Original) The circuit of Claim 1, further comprising a TVS array packaged in a SOIC-8 package.

15. (Original) The circuit of Claim 1, further comprising a TVS array packaged in an eight (8) pin dual-in-line package.

16. (Original) The circuit of Claim 1, further comprising a TVS array packaged in a SOIC-14 package.

17. (Original) The circuit of Claim 1, further comprising a TVS array packaged in a fourteen (14) pin dual-in-line package.

18. (Original) The circuit of Claim 1, further comprising a TVS array provided in multiple discrete semiconductor chips.

19. (Original) The circuit of Claim 1, further comprising a TVS array using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

20. (Original) The circuit of Claim 1, further comprising a TVS array using three (3) or more terminal packages containing multiple diodes within a single package where at least one of the diodes is a TVS.

21. (Original) The circuit of Claim 1, adapted for use in high frequency telecommunication lines.

22. (Original) The circuit of Claim 1, adapted for use in wireless communications devices.

23. (Original) The circuit of Claim 1, adapted for use in high baud-rate lines requiring TVS protection.

24. (Original) The circuit of Claim 1, adapted for use in multimedia systems.

25. (Original) The circuit of Claim 1, adapted for use in network applications and system designs.